

PCI-Bus Hot Swap Controller

September 1998

FEATURES

- Allows Safe Board Insertion and Removal from a Live PCI Slot
- Works on either a Motherboard or CompactPCI™ Card
- Controls –12V, 3.3V, 5V, 12V Supplies
- Programmable Fold-Back Current Limit with Circuit Breaker
- User-Programmable Supply Voltage Power-Up Rate
- High Side Drive for External N-Channels
- –12V and 12V On-Chip Switches
- Fault and Power-Good Outputs

APPLICATIONS

- PCI-Based Servers
- CompactPCI Compliant Boards

DESCRIPTION

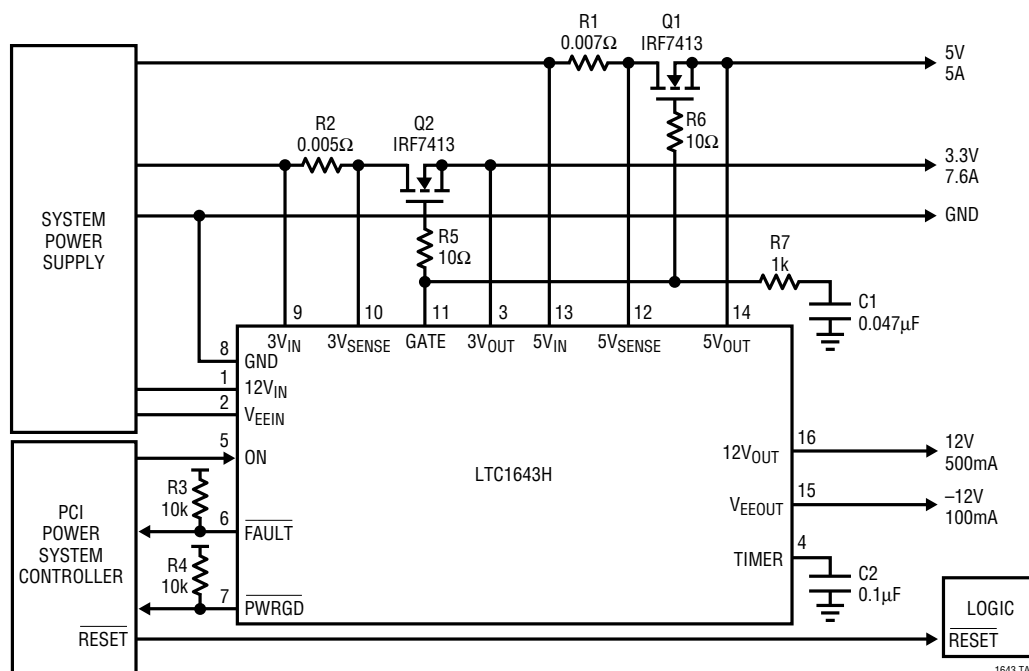
The LTC®1643 is a Hot Swap™ controller that allows a board to be safely inserted and removed from a live PCI-Bus slot. Two external N-channel transistors control the 3.3V and 5V supplies while on-chip switches control the –12V and 12V supplies. All supply voltages can be ramped up at a programmable rate. An electronic circuit breaker protects all four supplies against overcurrent faults. The fold-back current limit feature limits current spikes and power dissipation when shorts occur and allows boards with large capacitances to be powered up without tripping the circuit breaker. The $\overline{\text{PWRGD}}$ output indicates when all of the supply voltages are within tolerance and the $\overline{\text{FAULT}}$ output indicates an overcurrent condition. The ON(LTC1643H)/ $\overline{\text{ON}}$ (LTC1643L) pin is used to cycle the board power or reset the circuit breaker.

The LTC1643 is available in a 16-pin narrow SSOP package.

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TYPICAL APPLICATION

Hot Swappable PCI Supply



LTC1643L/LTC1643H

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

12V_{IN} 13.2V

V_{EEIN} -13.2V

Input Voltage (Pin 5) -0.3V to (12V_{IN} + 0.3V)

Output Voltages (Pins 6, 7) -0.3V to (12V_{IN} + 0.3V)

Analog Voltages

(Pins 3, 4, 9, 10 to 14) -0.3V to (12V_{IN} + 0.3V)

V_{EEOUT} -13.2V to +0.3V

12V_{OUT} -0.3V to 13.2V

Operating Temperature Range

Commercial 0°C to 70°C

Industrial -45°C to 85°C

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
12V _{IN}	1	16 12V _{OUT}
V _{EEIN}	2	15 V _{EEOUT}
3V _{OUT}	3	14 5V _{OUT}
TIMER	4	13 5V _{IN}
ON/ON*	5	12 5V _{SENSE}
FAULT	6	11 GATE
PWRGD	7	10 3V _{SENSE}
GND	8	9 3V _{IN}
GN PACKAGE 16-LEAD NARROW PLASTIC SSOP		LTC1643HCGN LTC1643LCGN LTC1643HIGN LTC1643LIGN
* ON FOR LTC1643H, $\overline{\text{ON}}$ FOR LTC1643L		
T _{JMAX} = 150°C, θ_{JA} = 135°C/W		

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{12VIN} = 12V, V_{EE} = -12V, V_{3VIN} = 3.3V, V_{5VIN} = 5V, T_A = 25°C (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{DD}	V _{12VIN} Supply Current	ON = 3V, ON = GND	●	3.5	8	mA
V _{LKO}	Undervoltage Lockout	12V _{IN}	●	7	9	V
		3V _{IN}	●	2.25	2.5	V
		5V _{IN}	●	2.25	2.5	V
V _{FB}	Fold-Back Current Limit Voltage	V _{FB} = (V _{5VIN} - V _{5VSENSE}), V _{5VOUT} = 0V	●	4	7.5	mV
		V _{FB} = (V _{5VIN} - V _{5VSENSE}), V _{5VOUT} > 2.5V	●	40	53	mV
		V _{FB} = (V _{3VIN} - V _{3VSENSE}), V _{3VOUT} = 0V	●	4	7.5	mV
		V _{FB} = (V _{3VIN} - V _{3VSENSE}), V _{3VOUT} > 1.3V	●	40	53	mV
t _{CB}	Circuit Breaker Trip Filter Time			15		μs
I _{CP}	GATE Pin Output Current	Charge Pump On, V _{GATE} = GND, FAULT = High	●	-20	-50	μA
		Charge Pump Off, V _{GATE} = 5V, FAULT = High		200		μA
		Charge Pump Off, V _{GATE} = 5V, FAULT = Low	●	3	10	mA
ΔV _{GATE}	External Gate Voltage	(V _{12VIN} - V _{GATE})		100	200	mV
V _{DROP}	Internal Switch Voltage Drop	(V _{12VIN} - V _{12VOUT}), I = 500mA	●	250	600	mV
		C Grade	●	250	750	mV
		I Grade	●	120	250	mV
		(V _{EEOUT} - V _{EEIN}), I _{EE} = 100mA	●			
I _{CL}	Current Fold-Back	12V _{IN} , 12V _{OUT} = 0V	●	50	250	mA
		12V _{IN} , 12V _{OUT} = 12V	●	525	850	mA
		V _{EEIN} , V _{EEOUT} = 0V	●	100	160	mA
		V _{EEIN} , V _{EEOUT} = -12V	●	225	450	mA
T _{TS}	Thermal Shutdown Temperature			150		°C
V _{TH}	Power-Good Threshold Voltage	V _{12VOUT}	●	10.8	11.1	V
		C Grade	●	10.4	11.1	V
		I Grade	●			
		V _{EEOUT}	●	-10.2	-10.5	V
		C Grade	●	-10.0	-10.5	V
		I Grade	●			
		V _{3VOUT}	●	2.8	2.9	V
		C Grade	●	2.75	2.9	V
		I Grade	●			
		V _{5VOUT}	●	4.5	4.65	V
		C Grade	●	4.4	4.65	V
		I Grade	●			

DC ELECTRICAL CHARACTERISTICS $V_{12VIN} = 12V$, $V_{EE} = -12V$, $V_{3VIN} = 3.3V$, $V_{5VIN} = 5V$, $T_A = 25^\circ C$ (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{IL}	Input Low Voltage	ON/ \overline{ON} , \overline{FAULT}	●			0.8	V
V _{IH}	Input High Voltage	ON/ \overline{ON} , \overline{FAULT}	●	2			V
V _{OL}	Output Low Voltage	\overline{FAULT} , PWRGD, I = 3mA	●			0.4	V
I _{IN}	ON/ \overline{ON} Pin Input Current	ON/ \overline{ON} = GND ON/ \overline{ON} = 12V _{IN}	● ●		±0.08 ±0.08	±10 ±10	μA μA
	5V _{SENSE} Input Current	5V _{SENSE} = 5V	●		50	100	μA
	3V _{SENSE} Input Current	3V _{SENSE} = 3V	●		50	100	μA
	5V _{IN} Input Current	5V _{IN} = 5V	●		460	700	μA
	3V _{IN} Input Current	3V _{IN} = 3V	●		320	600	μA
	5V _{OUT} Input Current	5V _{OUT} = 5V, \overline{ON} = 3V, ON = GND	●		240	500	μA
	3V _{OUT} Input Current	3V _{OUT} = 3V, \overline{ON} = 3V, ON = GND	●		220	500	μA
R _{DIS}	5V _{OUT} Discharge Impedance	ON = GND or \overline{ON} = 3V			100		Ω
	3V _{OUT} Discharge Impedance	ON = GND or \overline{ON} = 3V			70		Ω
	12V _{OUT} Discharge Impedance	ON = GND or \overline{ON} = 3V			450		Ω
	V _{EEOUT} Discharge Impedance	ON = GND or \overline{ON} = 3V			1600		Ω
I _{TIMER}	TIMER Pin Current	Timer On, V _{TIMER} = GND Timer Off, V _{TIMER} = 5V	●	−15	−22 45	−27	μA mA
V _{TIMER}	TIMER Threshold Voltage	(V _{12VIN} − V _{TIMER})	●	0.5	0.9	1.3	V

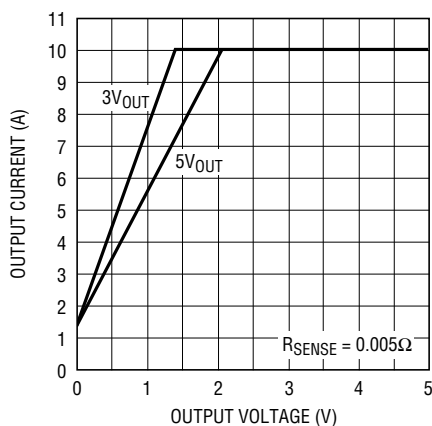
The ● denotes specifications that apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are reference to ground unless otherwise specified.

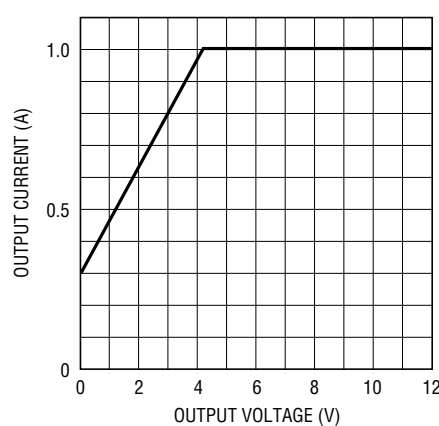
TYPICAL PERFORMANCE CHARACTERISTICS

3.3V and 5V Current Fold-Back Profile



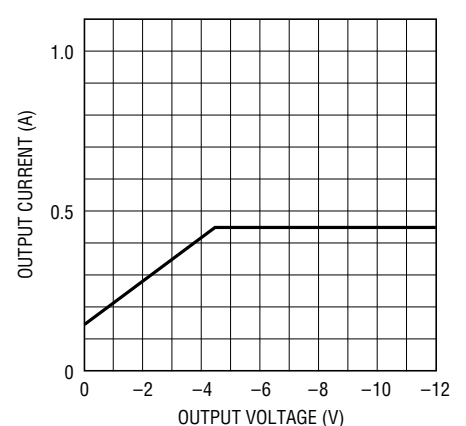
1643 G01

12V Current Fold-Back Profile



1643 G02

-12V Current Fold-Back Profile



1643 G03

PIN FUNCTIONS

12V_{IN} (Pin 1): 12V Supply Input. It powers all the chip's internal circuitry. A 0.5Ω switch is connected between 12V_{IN} and 12V_{OUT} with a fold-back current limit. An undervoltage lockout circuit prevents the switches from turning on while the 12V_{IN} pin voltage is less than 9V.

V_{EEIN} (Pin 2): -12V Supply Input. A 1.2Ω switch is connected between V_{EEIN} and V_{EEOUT} with a fold-back current limit.

3V_{OUT} (Pin 3): Analog Input. Used to monitor the 3.3V output supply voltage. The PWRGD signal cannot go high until the 3V_{OUT} pin exceeds 3V.

TIMER (Pin 4): Analog Current Fault Inhibit Timing Input. Connect a capacitor from TIMER to GND. With the chip turned off (ON = GND or $\overline{\text{ON}}$ = High) or the internal circuit breaker tripped ($\overline{\text{FAULT}}$ = GND), the TIMER pin is internally held at GND. When the chip is turned on, a $20\mu\text{A}$ pull-up current source is connected to TIMER. Current limit faults will be ignored until the voltage at the TIMER pin rises to within 0.9V of 12V_{IN}.

ON/ $\overline{\text{ON}}$ (Pin 5): Digital Input. The LTC1643L has an active low enable, $\overline{\text{ON}}$, and the LTC1643H has an active high enable, ON. When the ON pin is pulled high or the $\overline{\text{ON}}$ pin pulled low, the GATE pin is pulled high by a $50\mu\text{A}$ current source and the internal 12V and -12V switches are turned on. When the ON pin is pulled low or the $\overline{\text{ON}}$ pin pulled high, the GATE pin will be pulled to ground by a $200\mu\text{A}$ current source and the 12V and -12V switches turned off.

The ON/ $\overline{\text{ON}}$ pin is also used to reset the electronic circuit breaker. If the ON/ $\overline{\text{ON}}$ pin is cycled following the trip of the circuit breaker, the circuit breaker is reset and a normal power-up sequence will occur.

FAULT (Pin 6): Open-Drain Digital I/O. $\overline{\text{FAULT}}$ is pulled low when a current limit fault is detected. Current limit faults are ignored while the voltage at the TIMER pin is less than 12V_{IN} - 0.9V. Once the TIMER cycle is complete, $\overline{\text{FAULT}}$ will pull low $15\mu\text{s}$ after any of the supplies go into current limit. At the same time the GATE and TIMER pins are pulled to GND and the 12V and -12V switches are turned off. The chip will remain latched in the off state until the ON/ $\overline{\text{ON}}$ pin is toggled or the power is cycled.

Forcing the $\overline{\text{FAULT}}$ pin low with an external pull-down will immediately turn off the internal switches and force the GATE and TIMER pins to GND independent of the state of the ON/ $\overline{\text{ON}}$ pin. However, the chip is not latched into the off state, so when the $\overline{\text{FAULT}}$ pin is released, the state of the chip will be determined by the ON pin.

PWRGD (Pin 7): Open-Drain Digital Power-Good Output. PWRGD remains low while $V_{12\text{VOUT}} \geq 11.4\text{V}$, $V_{3\text{VOUT}} \geq 3\text{V}$, $V_{5\text{VOUT}} \geq 4.75\text{V}$ and $V_{\text{EEOUT}} \leq -10.8\text{V}$. When one of the supplies falls below its power-good threshold voltage, PWRGD will go high after a $15\mu\text{s}$ deglitching time. The switches will *not* be turned off when PWRGD goes high.

GND (Pin 8): Chip Ground.

3V_{IN} (Pin 9): 3.3V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the 3V_{IN} pin is less than 2.5V. If no 3.3V input supply is available, tie 3V_{IN} to the 5V_{IN} pin.

3V_{SENSE} (Pin 10): The 3.3V Current Limit Set Pin. With a sense resistor placed in the supply path between 3V_{IN} and 3V_{SENSE}, the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch. A fold-back feature makes the current limit decrease as the voltage at the 3V_{OUT} pin approaches GND. To disable the current limit, 3V_{SENSE} and 3V_{IN} can be shorted together.

GATE (Pin 11): High Side Gate Drive for the External N-Channels. Requires an external series RC network for the current limit loop compensation and setting the minimum ramp-up rate. During power-up, the slope of the voltage rise at the GATE is set by the $50\mu\text{A}$ current source connected to 12V_{IN} and the external capacitor connected to GND or by the 3.3V or 5V current limit and the bulk capacitance on the 3V_{OUT} or 5V_{OUT} supply lines. During power-down, the slope of the falling voltage is set by the $200\mu\text{A}$ current source connected to GND and the external GATE capacitor.

The voltage at the GATE pin will be modulated to maintain a constant current with either the 3V or 5V supplies go into current limit. When a current limit fault occurs after the inhibit period set by the TIMER pin capacitance, the undervoltage lockout circuit on 3.3V, 5V or 12V trips or

PIN FUNCTIONS

the $\overline{\text{FAULT}}$ pin is pulled low, the GATE pin is immediately pulled to GND.

5V_{SENSE} (Pin 12): 5V Current Limit Set Pin. With a sense resistor placed in the supply path between 5V_{IN} and 5V_{SENSE}, the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch. A fold-back feature makes the current limit decrease as the voltage at the 5V_{OUT} pin approaches GND. To disable the current limit, 5V_{SENSE} and 5V_{IN} can be shorted together.

5V_{IN} (Pin 13): Analog Input. Used to monitor the 5V input supply voltage. An undervoltage lockout circuit prevents

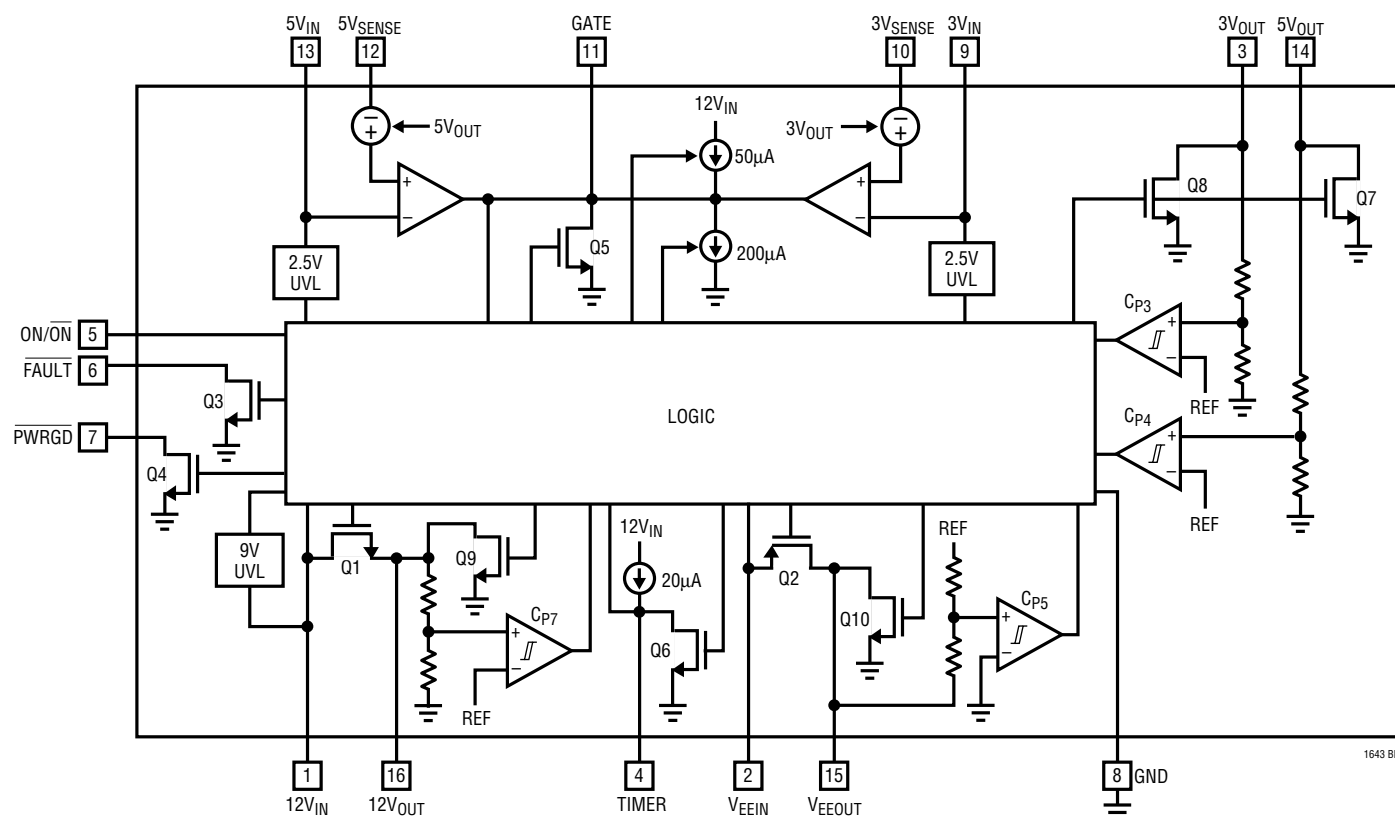
the switches from turning on when the voltage at the 5V_{IN} pin is less than 2.5V.

5V_{OUT} (Pin 14): Analog Input. Used to monitor the 5V output supply voltage. The PWRGD signal cannot go high until the 5V_{OUT} pin exceeds 4.75V.

V_{EEOUT} (Pin 15): –12V Supply Output. A 1.2Ω switch is connected between V_{EEIN} and V_{EEOUT}. V_{EEOUT} must exceed –10.8V before the PWRGD signal can go high.

12V_{OUT} (Pin 16): 12V Supply Output. A 0.5Ω switch is connected between 12V_{IN} and 12V_{OUT}. 12V_{OUT} must exceed 11.4V before the PWRGD signal can go high.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Hot Circuit Insertion

When a circuit board is inserted into a live PCI slot, the supply bypass capacitors on the board can draw huge transient currents from the PCI power bus as they charge up. The transient currents can cause permanent damage to the connector pins and cause glitches on the power bus, causing other boards in the system to reset.

The LTC1643 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live PCI slot without glitching the system power supplies. The chip also protects the PCI supplies from shorts and monitors the supply voltages.

The LTC1643H is designed for motherboard applications, while the LTC1643L is designed for CompactPCI applications where the chip resides on the plug-in board.

LTC1643 FEATURE SUMMARY

1. Allows safe board insertion and removal from either a motherboard (LTC1643H) or CompactPCI board (LTC1643L).
2. Controls all four PCI supplies: -12V, 12V, 3.3V and 5V.
3. Programmable fold-back current limit: a programmable analog current limit with a value that depends on the output voltage. If the output is shorted to ground, the current limit drops to keep power dissipation and supply glitches to a minimum.
4. Programmable circuit breaker: if a supply remains in current limit too long, the circuit breaker will trip, the supplies will be turned off and the FAULT pin pulled low.

5. Current limit power-up: the supplies are allowed to power up in current limit. Allows the chip to power up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is programmable using the TIMER pin.
6. -12V and 12V power switches on chip.
7. Power good output: monitors the voltage status of the four supply voltages.
8. Space saving 16-pin SSOP package.

PCI Power Requirements

PCI systems usually require four power rails: 5V, 3.3V, 12V and -12V. Systems implementing the 3.3V signaling environment are usually required to provide all four rails in every system. Systems implementing the 5V signaling environment may either ship the 3.3V supply with the system or provide a means to add it afterward. The tolerance of the supplies as measured at the components on the plug-in card is summarized in Table 1.

Table 1. PCI Power Supply Requirements

SUPPLY	TOLERANCE	CAPACITIVE LOAD
5V	5V \pm 5%	<3000 μ F
3.3V	3.3V \pm 0.3V	<3000 μ F
12V	12V \pm 5%	<500 μ F
-12V	-12V \pm 10%	<120 μ F

APPLICATIONS INFORMATION

Power-Up Sequence

The power supplies are controlled by placing external N-channel pass transistors in the 3.3V and 5V power paths, and internal pass transistors for the 12V and -12V power paths (Figure 1).

Resistors R1 and R2 provide current fault detection and R7 and C1 provide current control loop compensation. Resistors R5 and R6 prevent high frequency oscillations in Q1 and Q2.

When the ON pin (Pin 5) is pulled high, the pass transistors are allowed to turn on and a 20 μ A current source is connected to the TIMER pin (Pin 4) (Figure 2).

The current in each pass transistor increases until it reaches the current limit for each supply. Each supply is then allowed to power up at the rate $dv/dt = 50\mu A/C1$ or as determined by the current limit and the load capacitance whichever is slower. Current limit faults are ignored while the TIMER pin (Pin 4) voltage is ramping up and is less than 0.9V below 12V_{IN} (Pin 1). Once all four supply voltages are within tolerance, the PWRGD pin (Pin 7) will pull low.

Power-Down Sequence

When the ON (Pin 5) is pulled low, a power-down sequence begins (Figure 3).

Internal switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The TIMER pin (Pin 4) is immediately pulled low. The GATE pin (Pin 11) is pulled down by a 200 μ A current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously and glitching the power supply voltages. When any of the output voltages dip below its threshold, the PWRGD pin (Pin 7) pulls high.

Timer

During a power-up sequence, a 20 μ A current source is connected to the TIMER pin (Pin 4) and current limit faults are ignored until the voltage ramps to within 0.9V of 12V_{IN} (Pin 1). This feature allows the chip to power up a PCI slot that can accept boards with widely varying capacitive loads on the supplies. The power-up time will be:

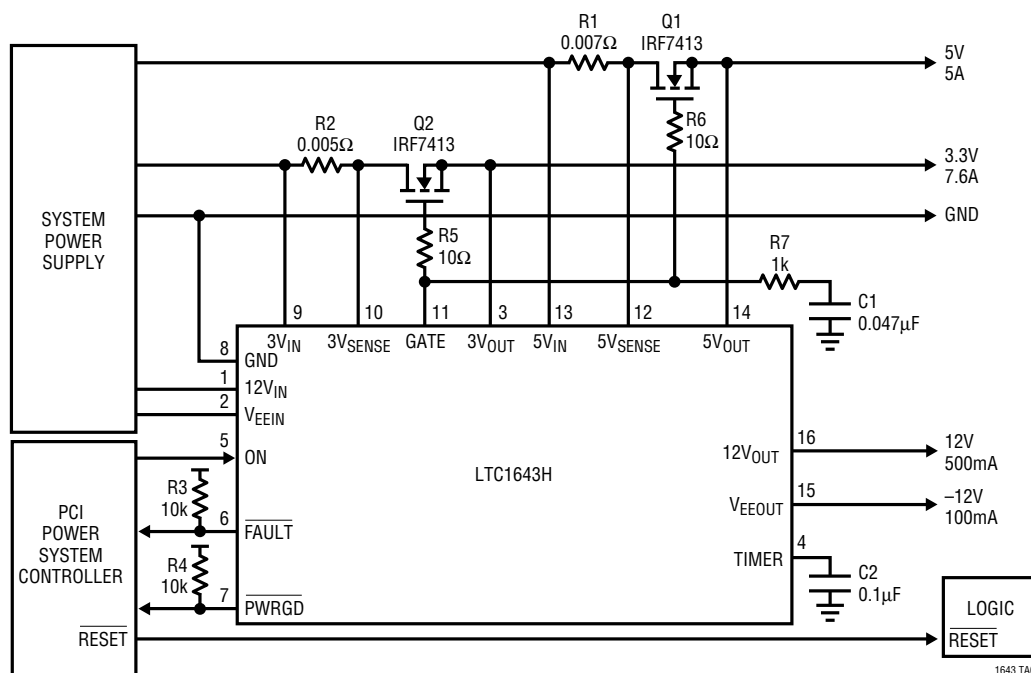


Figure 1. Typical Application

APPLICATIONS INFORMATION

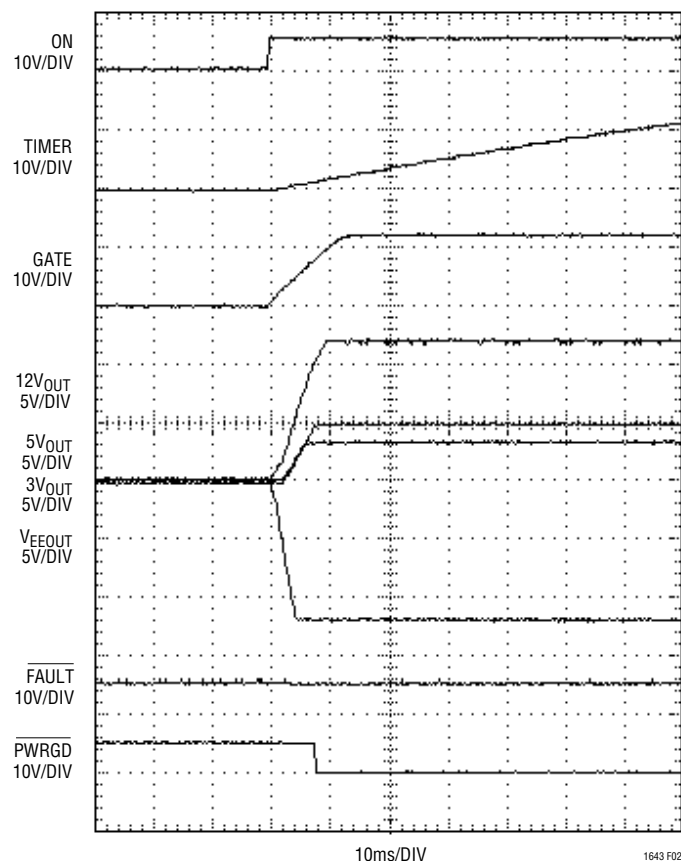


Figure 2. Normal Power-Up Sequence

$$t_{ON} \cong 2 \frac{C_{SUPPLY} \cdot V_{SUPPLY}}{I_{LIMIT} - I_{LOAD}}$$

For $C_{SUPPLY} = 2000\mu F$, $V_{SUPPLY} = 5V$, $I_{LIMIT} = 7A$, $I_{LOAD} = 5A$, the turn-on time will be $\sim 10ms$. The timer period should be set longer than the maximum supply turn-on time but short enough to not exceed the maximum safe operating area of the pass transistor during a short circuit. The timer period will be:

$$t_{TIMER} = \frac{C_{TIMER} \cdot 11.1V}{22\mu A}$$

For $C_{TIMER} = 0.1\mu F$, the timer period will be $\sim 50ms$. The TIMER pin (Pin 4) is immediately pulled low when ON (Pin 5) goes low.

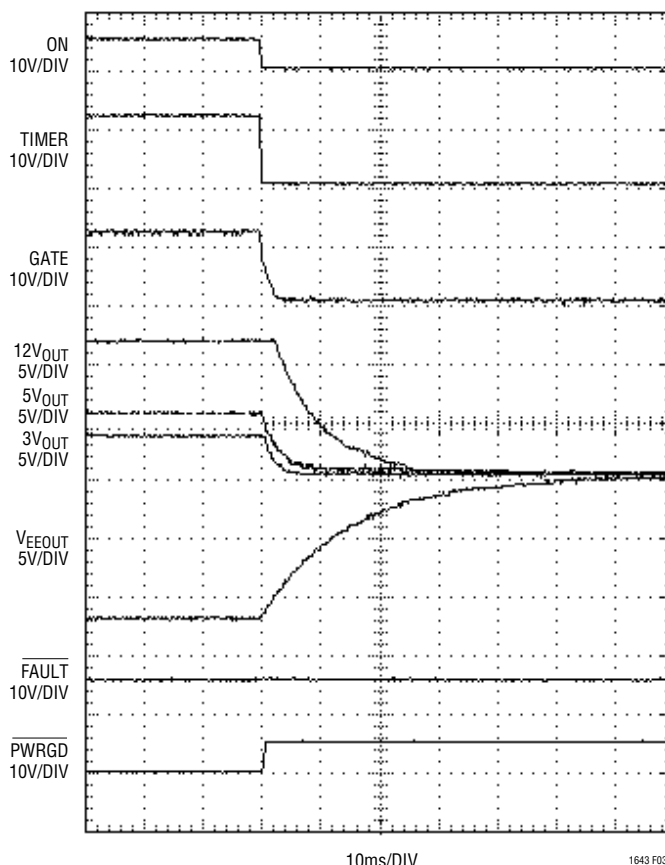


Figure 3. Normal Power-Down Sequence

Thermal Shutdown

The internal switches for the 12V and $-12V$ supplies are protected by an internal current limit and thermal shutdown circuit. When the temperature of chip reaches $150^{\circ}C$, all switches will be latched off and the FAULT pin (Pin 6) will be pulled low.

Short-Circuit Protection

During a normal power-up sequence, if the TIMER (Pin 4) is done ramping and a supply is still in current limit, all of the pass transistors will be immediately turned off and the FAULT pin (Pin 6) will be pulled low as shown in Figure 4.

If a short circuit occurs after the supplies are powered up, the shorted supply's current will drop immediately to the limit value (Figure 5).

APPLICATIONS INFORMATION

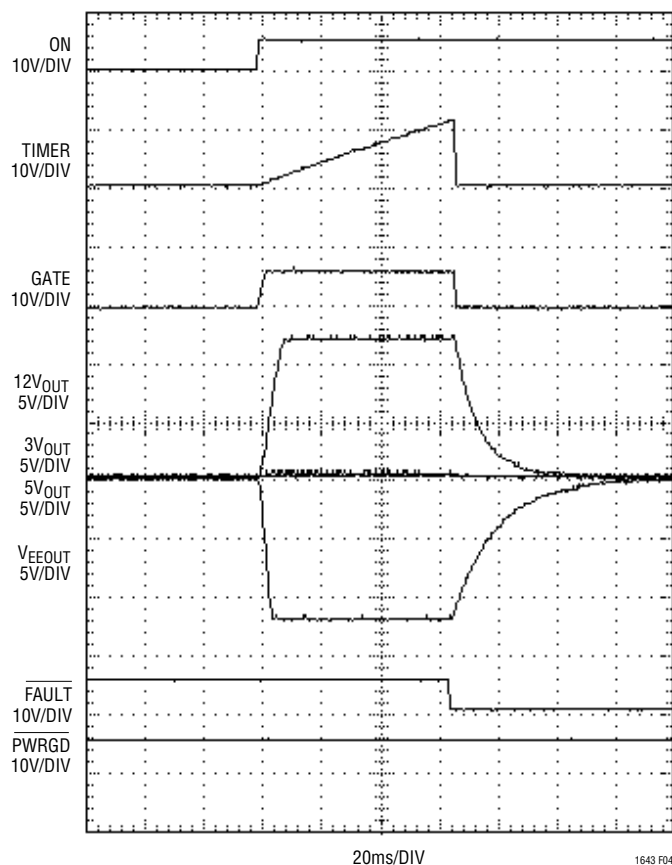


Figure 4. Power-Up into a Short on 3.3V Output

If the supply remains in current limit for more than 15 μ s, all of the supplies will be latched off. The 15 μ s delay prevents quick current spikes—for example, from a fan turning on—from causing false trips of the circuit breaker. The chip will stay in the latched-off state until ON (Pin 5) is cycled low then high, or the 12VIN pin (Pin 1) power supply is cycled.

To prevent excessive power dissipation in the pass transistors and to prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function where huge currents can flow before the breaker trips, the current fold-back feature assures that the supply current will be kept at

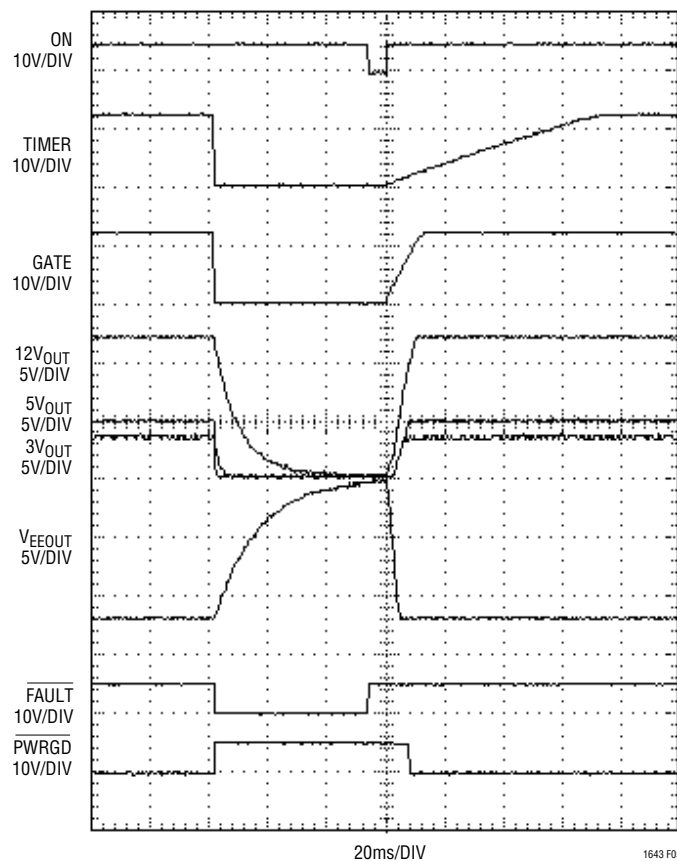


Figure 5. Short Circuit on 5V

a safe level and prevent voltage glitches when powering up into a short.

The current limit for the 5V and 3.3V supplies is set by placing a sense resistor between 5VIN (Pin 13) and 5VSENSE (Pin 12) and between 3VIN (Pin 9) and 3VSENSE (Pin 10). The current limit will be set by:

$$I_{LIMIT} = 53\text{mV}/R_{SENSE}$$

For a 0.005 Ω resistor, the current limit will be set at 10.6A and fold back to 1.5A when the output is shorted. For a 0.007 Ω resistor, the current limit will be set at 7.6A and fold back to 1.1A when the output is shorted.

The current for the internal 12V switch is set at 850mA folding back to 250mA and the -12V switch at 450mA folding back to 160mA.

APPLICATIONS INFORMATION

CompactPCI Application

The LTC1643L is ideal for hot swapping CompactPCI boards. The typical application is shown in Figure 6. Because the turn-on signal is active low for CompactPCI, the LTC1643L must be used. Capacitors C3 and C4 are required when hot-plugging the chip into a live backplane.

Systems Without 3.3V

If a system does not use a 3.3V supply, the LTC1643 should be connected as shown in Figure 7.

Increasing 12V and -12V Current Capability

The internal switches in the LTC1643 are designed for up to 500mA loads on 12V and 200mA on -12V. If more current is needed, then the circuits in Figure 8 can be used.

For the 12V supply, P-channel transistor Q4 is placed in parallel with the internal switch. When the LTC1643H is turned off, the GATE pin is held low and transistor Q3 is turned on which pulls the gate of Q4 high, turning it off. When the LTC1643H is turned on, the GATE pin goes high, turning off Q3 and allowing R8 to pull the gate of Q4 low to turn it on.

Because Q4 is in parallel with the internal 12V switch, the load current will be shared in proportion to their respective $R_{DS(ON)}$ values. For example, if the $R_{DS(ON)}$ of the external switch is 0.2Ω and the internal switch is 0.4Ω , then, at 1.5A load current, the external switch will provide 1A and the internal switch 500mA. The circuit breaker current will be reached when the internal current reaches 1A and the external current is 2A or 3A load current.

For the -12V supply, N-channel transistor Q6 is used to provide the extra load current. When the LTC1643H is turned on, the internal V_{EE} switch is turned on and the -12V output starts to pull down through D1 and turns on Q5. When Q5 turns on, the gate of Q6 starts to rise, turning it on. When the LTC1643H turns off, the V_{EEOUT} pin is pulled up to ground, diode D1 is reversed biased, and transistor Q5 turns off, which allows resistor R10 to turn off Q6.

The internal -12V switch provides the current limit for the supply, but because the high $R_{DS(ON)}$ of the internal switch (1.2Ω) is in series with D1, very large currents can flow through Q6 before the circuit breaker trips. However, if a short to ground occurs on the -12V output, diode D1 will prevent Q5 from turning on, which will prevent Q6 from turning on.

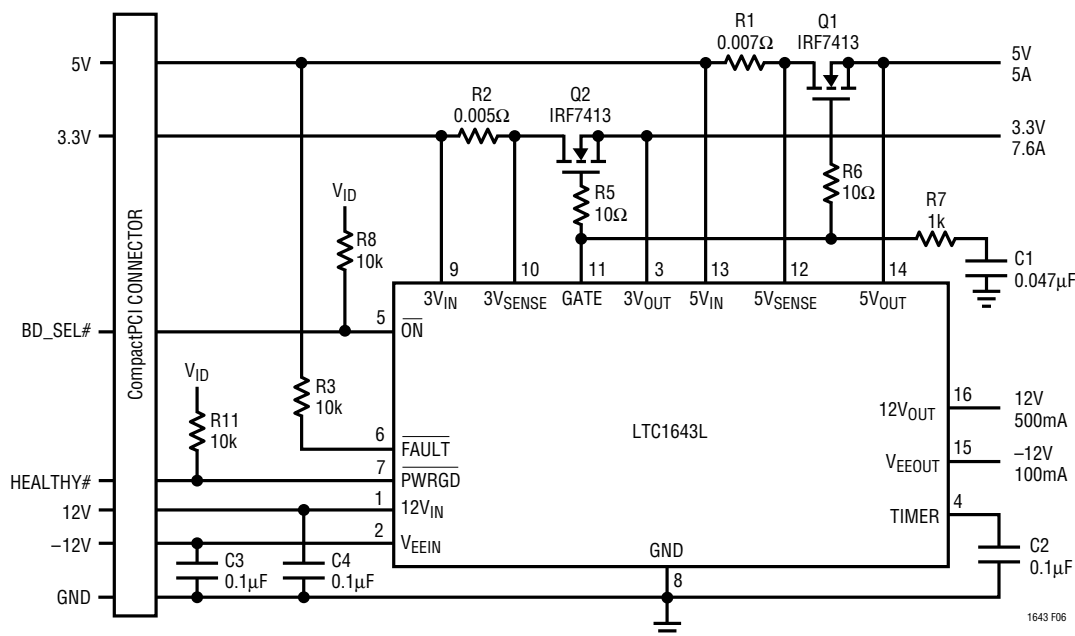


Figure 6. Typical CompactPCI Application

APPLICATIONS INFORMATION

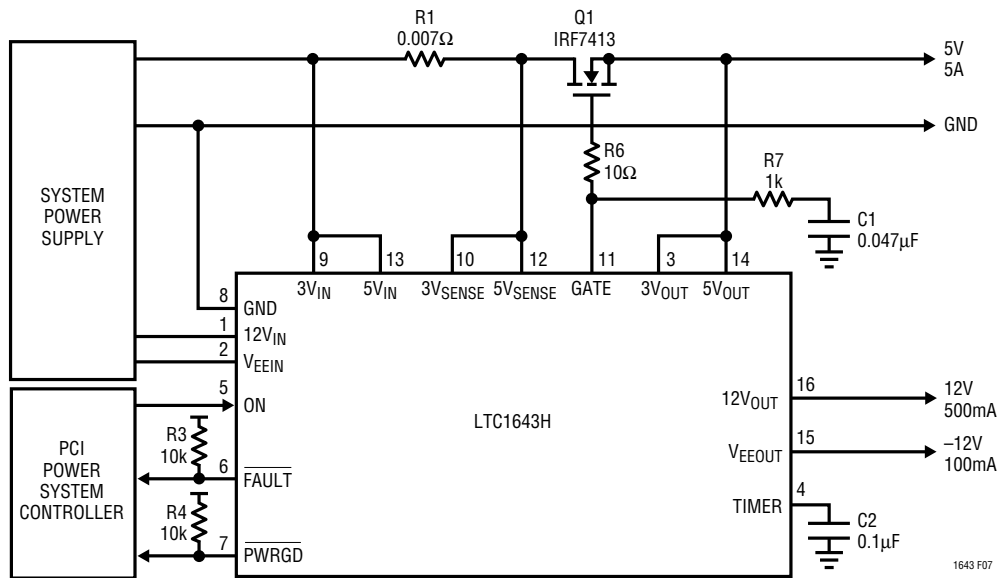


Figure 7. System Without 3.3V Supply

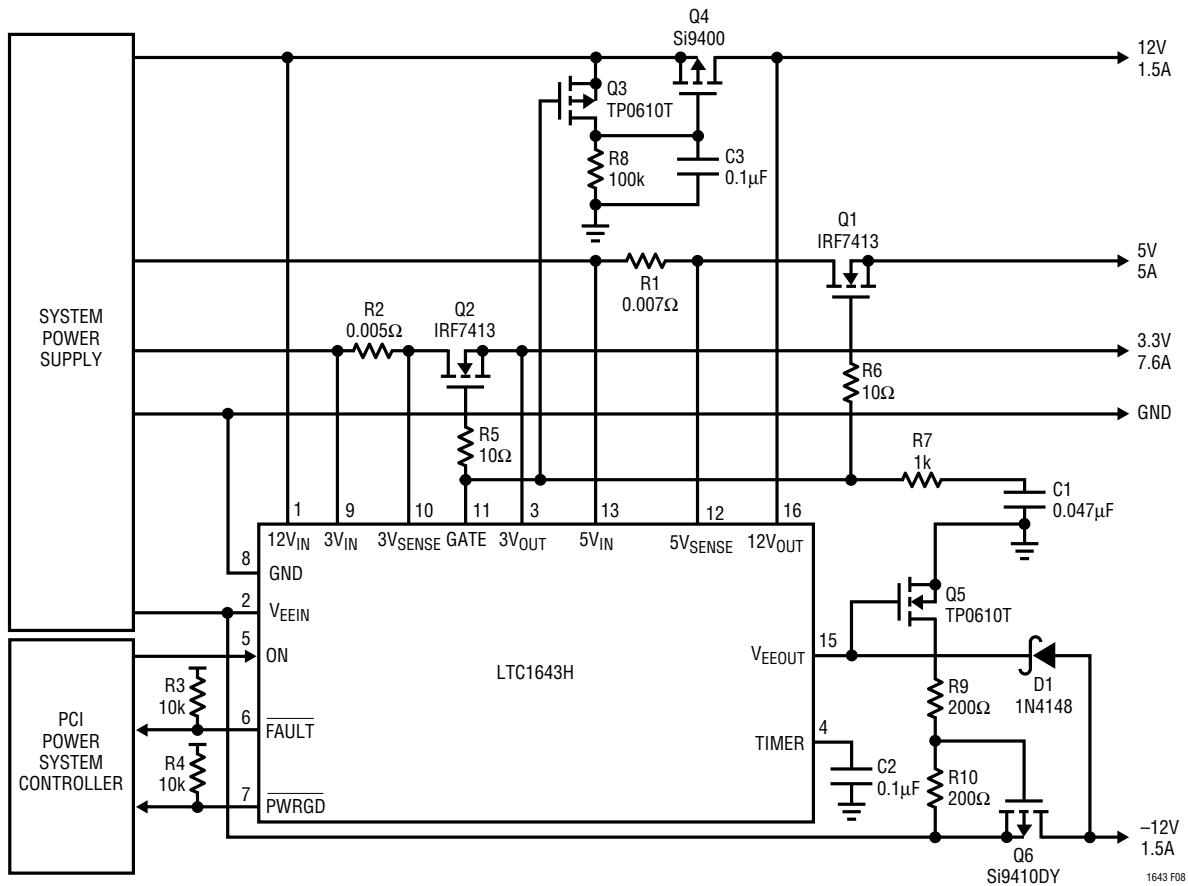
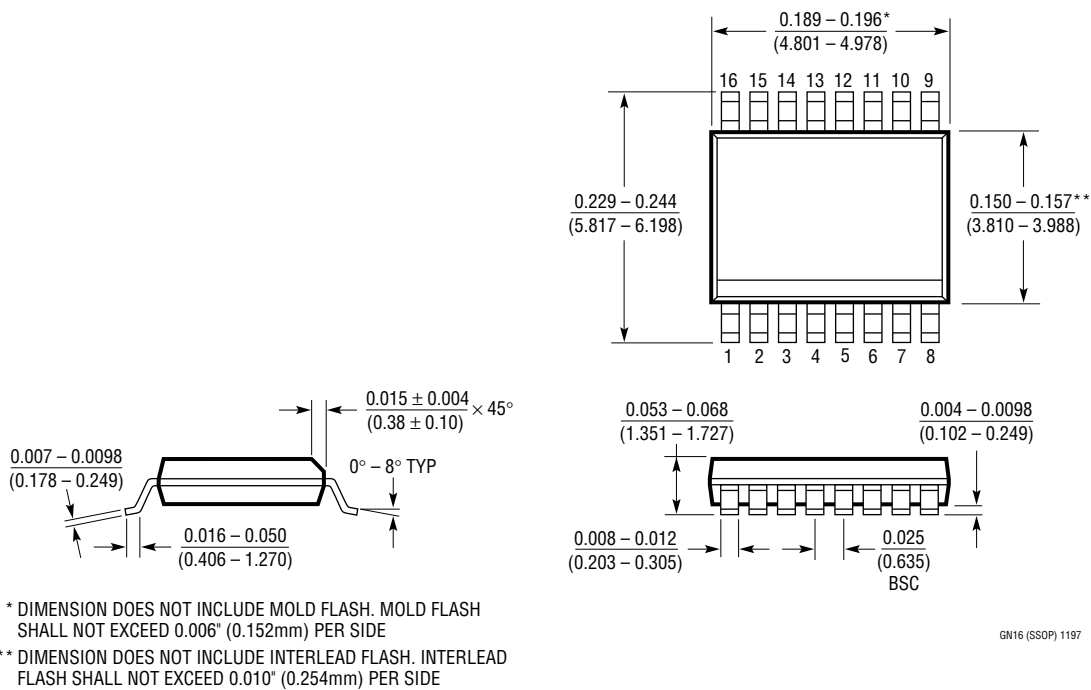


Figure 8. Increasing 12V and -12V Current Capability

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Hot Swap Controller	Multiple Supply
LTC1422	Hot Swap Controller	Single Supply
LT1640	-48V Hot Swap Controller	Negative High Voltage Supplies